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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
	)	
Michio Asahina	)	Group Art Unit: 258
	)	
Serial No.: 07/151,361	)	Examiner: S. Loke
	)	
Filed: February 2, 1988	)	
	)	
For: SEMICONDUCTOR DEVICE	)	

91-2458

APPELLANT'S BRIEF ON APPEAL

This is an Appeal from a final rejection which issued on November 20, 1989. Petitions for Extensions of Time of two months have been filed, and the formal Notice of Appeal was filed on April 20, 1990.

STATUS OF CLAIMS

The application contains claims 1-22, which are all of the claims that were originally filed, and all of which are appealed.

STATUS OF AMENDMENTS

No amendments were requested subsequent to final rejection.

SUMMARY OF THE INVENTION

The present invention relates to the manufacture of integrated semiconductor circuits composed of a plurality of layers which may variously be insulating, semiconductive or conductive. It has been found that in structures of this type which are manufactured according to the prior art, flaws in the form of protrusions or voids may be created in a conductive layer, or in a layer adjacent thereto. Examples of such flaws are shown in Figure 1 where aluminum layer 1008 possesses a protrusion 1010 and a void 1011, and passivation layer 1009 possesses a void 1012. Such flaws seriously impair the reliability of integrated semiconductor devices, particularly when such devices are manufactured to have very small dimensions. (Specification, page 3, l. 1-4 and page 6, l. 18-25).

Furthermore, with conventional Al conductive paths, it is impossible to prevent stress migration, in which strong

tensile stress remains in the conductive paths, associated with compressive stress in the adjacent passivation layer, thereby resulting in a creep diffusion phenomenon which causes burnout of the conductive paths.

Moreover, electro migration has already reached the limit of device reliability and conductive path material having high reliability is needed to allow a stable flow of high current levels. (Specification, page 7, l. 1-10).

Simply stated, the present invention is based on Appellant's discovery that these drawbacks can be prevented by forming the, or each, conductive layer of such a semiconductor device as an electroplated or electrolessly plated metal plating layer. (Specification, page 11, l. 13 and page 18, l. 14). When the metal layer or layers of an integrated semiconductor device are formed as electroplated or electrolessly plated layers, projections and voids are prevented (Specification, page 13, l. 3-4) and electromigration, stress migration and contact migration tendencies are substantially eliminated (Specification, page 16, l. 8-10).

According to the prior art, such conductive layers are formed by techniques such as sputtering, vapor deposition, etc. (Specification, page 3, l. 5-7). When a conductive layer is formed by electroplating or electroless plating, it is, at least on a microscopic scale, more homogeneous and therefore provides a more uniform coverage, resulting in a better step coverage at locations where openings have been formed in the underlying layer, as well as providing better adhesion to the underlying layer (Specification, page 19, l. 1-19).

ISSUES

ISSUE 1: Whether Claims 1-10, 13 and 20 are unpatentable under 35 U.S.C. §103 over McDavid in view of Howard.

ISSUE 2: Whether Claim 11 is unpatentable under 35 U.S.C. §103 over McDavid in view of Howard and Baudrant et al.

ISSUE 3: Whether Claims 12 and 17 are unpatentable under 35 U.S.C.§103 over McDavid in view of Howard and Sasaki.

ISSUE 4: Whether Claims 15 and 16 are unpatentable over McDavid in view of Sasaki and Howard.

ISSUE 5: Whether Claims 14, 18 and 19 are unpatentable over McDavid in view of Howard and Brasen.

ISSUE 6: Whether Claims 21 and 22 are unpatentable under 35 U.S.C.§103 over Sasaki in view of Howard.

ISSUE 7: Whether Claims 5-7, 10, 13 and 22 are unpatentable under 35 U.S.C. §112, second paragraph.

ARGUMENT

ISSUES 1-6

As concerns the prior art rejections, issues 1-6, there is, in effect, a single underlying issue: Whether it would be obvious, in view of the prior art, to provide a semiconductor device with an electroplated or electrolessly plated metal plating layer disposed on and adhering to a further layer which is of a metal, a metal silicide, a metal nitride, a metal carbide or a conductive oxide film. As has already been pointed out above, such a metal plating layer has been found to offer significant benefits compared to the prior art. Thus, as is stated at page 12, lines 14-15 of the specification, the provision of such a metal plating layer acts to prevent the appearance of projections such as shown at 1010 and 1116 in Figures 1 and 2 of the application drawing. As stated at page 13, lines 3-7 of the specification, the provision of such a metal plating layer additionally serves to prevent the appearance of voids such as shown at 1011, 1012, 1117 and 1219 in Figures 1-3 of the application drawing. As further stated in the specification, the provision of such a metal plating layer serves to substantially eliminate electromigration, stress migration and contact migration tendencies in a semiconductor device.

Of the applied references, the Examiner relies only on the U.S. Patent to Howard for prior art teachings relative to the metal layers of an integrated semiconductor device. Since the principal distinction between the present invention and the prior art resides in the nature of such metal layer of a semiconductor device, it is believed that only the Howard patent need be discussed in detail.

The Howard patent does not disclose or suggest the provision, in a semiconductor device, of a metal plating layer in the form of an electroplated or electrolessly plated layer, and the Examiner recognizes that the Howard patent does not present such a disclosure.

Specifically, the Examiner admits that Howard discloses a metal conductive layer formed above a nitride layer (Paper No. 11, page 2). Most specifically, the Examiner recognizes that Howard does not disclose an electroplated or electrolessly plated layer, and the Examiner seeks to justify the rejection by the assertion that what Howard teaches is "just another method to prevent void (crack) beside electroplating or electrolessly plating." (Idem).

Thus, appellant and the Examiner are in agreement that, with respect to this feature of devices according to the present invention, the metal plating layer defined in the claims of the present application is different from the corresponding layer disclosed by Howard.

However, appellant and the Examiner disagree as to (1) whether the disclosure of Howard provides an acceptable basis for rejecting the application claims, and (2) whether the layer structure disclosed by Howard represents simply another technique to prevent, inter alia, voids, or cracks.

Regarding the first point, it is submitted to be well recognized that a claim defines a patentable advance over the prior art if it includes any feature which is not taught by the prior art.

Indeed, a consistent line of decisions by both the courts and the Board of Patent Appeals and Interferences has established that an improved result is not a requisite of patentability and that in order to support a prior art rejection, evidence relating to each claimed feature must be provided.

One decision which relied on this principle was In re Freed, 165 U.S.P.Q. 570, 571 (C.C.P.A., 1970), where the application claimed a process in which two steps are performed simultaneously. The applied reference disclosed performing the two steps separately and both the Examiner and the Board of Appeals held that performing the two steps simultaneously was obvious in view of the disclosure of the reference. This holding was reversed by the Court, which indicated that "a determination of obviousness must be based on facts and not on

unsupported generalities." Freed was cited in In re Saether, 181 U.S.P.Q. 36, 40 (C.C.P.A., 1974), in which a holding by the Board that the difference between the claimed invention and the references represent merely "the physical requirements of the users" was reversed because, in the Court's view, some evidence in support of that decision must appear in the record.

In re Boe, et al., 184 U.S.P.Q. 38 (C.C.P.A., 1974) cited Saether in a case involving a claim which recited "filaments at least partly composed of a segmented elastomer" and in which the Examiner had not cited any reference showing segmented elastomer. The Examiner's rejection was reversed on the basis that it ignored a specific claim limitation.

Boe, et al., was, in turn, relied upon in Ex parte Murphy, et al., 217 U.S.P.Q. 479, 81 (Bd. of App., 1982). In this case, the application claim recited a hollowed spike of hard material fitted on the flanged end of the hollow stem of resilient material, and no prior art was cited to show such a structure. The Board stated that since all limitations of a claim must be considered in determining the claimed subject matter, and it is error to ignore specific limitations distinguishing over the reference, it is necessary that the modification of a prior art device to meet the claim be obvious from teachings in secondary references when taken in conjunction with the level of skill of those having ordinary skill in the art.

Similarly, in Ex parte Parthasarathy, et al., 174 U.S.P.Q. 63 (Bd. of App., 1971), the Board reversed the rejection, stating that nowhere in the record has the Examiner indicated any reason for finding obvious the alteration relative to the applied reference. In Ex parte Copping, 180 U.S.P.Q. 475, 76 (Bd. of App., 1972), the Board reversed the rejection, noting that the Examiner admits that limitations in the last three lines of the claim on appeal are not disclosed by the prior art, although the Examiner asserted that there has been no showing of an unobvious or improved result. The Board held that the prior art does not provide a factual basis to support a holding of obviousness.

In Ex parte Kaiser, 194 U.S.P.Q. 47 (Bd. of App., 1975), a claim was rejected even though the prior art did not disclose a claimed feature, which related to transistor emitter strips of different widths, the prior art disclosing strips of equal width. In reversing the rejection, the Board pointed out that

the absence of an improved result is not conclusive of unpatentability and that the Examiner had not advanced any factual reason for a finding of obviousness.

Also of interest is the decision In re Fine, 5 U.S.P.Q. 2d 1596, 1599 (C.A.F.C., 1988).

Applying these principles to the present case, each of claims 1 and 21 recites "an electroplated or electrolessly plated metal plating layer" disposed on and adhering to a previously recited layer, or formed in a through opening. The reference relied upon with respect to this feature, the U.S. Patent to Howard, discloses a layer which is not an electroplated or electrolessly plated metal plating layer. Thus, with regard to this feature, the Examiner has provided no evidence that it is known in the art, per se, or, more specifically, that it is known in the art to provide a conductive layer of a semiconductor device in the form of an electroplated or electrolessly plated metal plating layer. Therefore, the prior art rejections of record are not supported by the evidence relied upon by the Examiner.

Moreover, the present invention is based on appellant's discovery that a metal plating layer of the type defined in each of claims 1 and 21 produces unexpected improvements compared to conductive layers formed according to the teachings of Howard, which are formed by evaporation or sputtering.

The layers disclosed in the Howard reference are formed by depositing a material in the form of particles which form a layer analogous to a covering of snow, whereas electroplating or electrolessly plating results in the formation of a film which has a high degree of continuity and homogeneity. As a result, an electroplated or electrolessly plated layer creates a significantly greater degree of step coverage and adhesion to the underlying surface than can be achieved by evaporation or sputtering. The superior step coverage resulting from electroplating or electrolessly plating results in lower stress levels within the plating layer, with a substantially reduced tendency to form pores or voids. Moreover, the superior step coverage provided by such metal plating layers prevents atoms within the plating layer from concentrating at certain locations, resulting in a minimization of electromigration.

There is no basis in the prior art for the conclusion that the metal layers disclosed in the Howard patent will produce the improvements resulting from provision of metal

layers according to the present invention. Therefore, no basis exists for the assertion that the present invention represents simply another way of avoiding voids, or cracks, and protrusions.

Thus, since claims 2-20 depend from claim 1 and claim 22 depends from claim 21, the semiconductor devices defined in all of the claims of the present application have properties superior to devices fabricated according to the teachings of the prior art, including the teachings of Howard.

Accordingly, it is submitted that the prior rejections now of record cannot stand and it is therefore requested that these rejections be reconsidered and withdrawn.

Finally, note has been taken of the other references relied upon in the various rejections. Since, however, Howard is the only reference relied upon by the Examiner in connection with the feature asserted herein to distinguish over the prior art, a detailed discussion of the subject matter of the other references does not appear to be required.

ISSUE 7

Turning now to Issue 7, on page 3 of Paper No. 11, the Examiner rejects claims 5-7, 10, 13 and 22 under 35 U.S.C. § 112, second paragraph, as being indefinite, and further indicates that this is a restatement of a previous rejection. In particular, the Examiner asserts that the reason for this rejection was set forth in the first rejection, paper no. 9. Since applicant's copy of the previous rejection does not include a paper number, it must be assumed that the Examiner is referring to the Office Action mailed on June 6, 1989. However, in the Action of June 6, 1989, only claim 22 was rejected under 35 U.S.C. § 112, second paragraph; claims 5-7, 10 and 13 were rejected under 35 U.S.C. § 112, fourth paragraph, a ground of rejection distinctly different from one presented under the second paragraph.

In response to the rejection of claim 22 under 35 U.S.C. § 112, second paragraph, it was pointed out, in the amendment filed September 1, 1989, that claim 22 refers, in fact, to "said conductor structure component" and claim 21 recites only a single "conductor structure component". Since the Examiner has not commented on this response to the formal rejection of claim 22, counsel is unable to evaluate the basis for this continued rejection. As regards claims 5-7, 10 and 13, since

they were not previously rejected under 35 U.S.C. § 112, second paragraph, and the Examiner has not indicated why these claims are considered indefinite, counsel is unable to formulate a meaningful response to that rejection.

As concerns the formal rejection applied to those claims in the Office action of June 6, 1989, it can only be reiterated that the limitations appearing in these claims do further limit the structure of claim 1 in that claims 5, 6 and 7 each defines the metal plating layer in a manner which can be considered to be structural, the recitations in claim 10 further delimit the structure of the metal plating layer, and claim 13 is clearly directed to the composition of the metal plating layer. Indeed, for reasons advanced above, the fact is that a metal plating layer differs physically from the layer disclosed by Howard, from which it results that each of these claims does define a structural distinction over the prior art.

CONCLUSION

It will be seen from the above that, as regards the prior art rejections, Issues 1-6, the prior art relied upon by the Examiner does not provide evidence relating to at least one significant feature of the present invention, which is positively recited in the Claims. Furthermore, as regards Issue 7, the Claims in question do present a proper structural recitation of the contribution of the present invention.

It is accordingly requested that all of the rejections of Claims 1-22 be reversed and that the application be allowed.

The present brief is submitted in triplicate, togetherwith the Brief fee of $140.00 required by 37 C.F.R. §1.17 (f).

Respectfully submitted,

Dated June 20, 1990

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APPENDIX

1. A semiconductor device comprising:

a substrate having a doped semiconductor region, a gate wiring, a lower conductor structure, an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure, and an upper conductor structure connected to said lower conductor structure via said through opening, wherein said upper structure comprises: at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide or a conductive oxide film, and an electroplated or electrolessly plated metal plating layer disposed on and adhering to said at least one layer.

2. A device as defined in claim 1 wherein said at least one layer consists of a single layer.

3. A device as defined in claim 1 wherein said at least one layer comprises a combination of at least two layers, each said layer being of a respective one of said recited materials.

4. A device as defined in claim 1 wherein said metal plating layer comprises at least one of Cu, Ni, Au, Cr, Co, Rh, Pd and a solder material.

5. A device as defined in claim 4 wherein said metal plating layer is an electrolytically plated layer.

6. A device as defined in claim 4 wherein said metal plating layer is an electrolessly plated layer.

7. A device as defined in claim 1 wherein said metal plating layer comprises a combination of an electroplated layer and an electrolessly plated layer.

8. A device as defined in claim 1 wherein said metal plating layer comprises at least two alloy plating layers.

9. A device as defined in claim 1 wherein said metal plating layer comprises a superposed combination of a first plating layer composed of a single metal and a second plating layer composed of an alloy.

10. A device as defined in claim 1 wherein said metal plating layer is formed electrolytically by application of one of a direct current, an alternating current, an intermittent current and a periodically reversing current.

11. A device as defined in claim 1 wherein said doped semiconductor region is an impurity doped Si monocrystalline region.

12. A device as defined in claim 1 wherein said metal plating layer is disposed only within said through opening.

13. A device as defined in claim 12 wherein said metal plating layer is an electrolessly deposited layer of Cu, Ni, Au, Cr, Rh, Pd, or soldering material.

14. A device as defined in claim 13 wherein said metal plating layer conductively connects at least one of said gate wiring and said lower conductor structure to said upper conductor structure.

15. A device as defined in claim 12 wherein said metal plating layer a plurality of superposed layers of respectively different materials.

16. A device as defined in claim 12 wherein said metal plating layer is composed of an alloy.

17. A device as defined in claim 1 wherein said gate wiring and said lower conductor structure are composed of a conductive layer of polysilicon, metal silicide, metal polycide, refractory metal, or a metal of the Al series.

18. A device as defined in claim 17 wherein said gate wiring and said lower conductor structure further comprise a metal plating layer deposited on said conductive layer.

19. A device as defined in claim 17 wherein said metal plating layer is formed at said gate wiring and said lower conductor structure.

20. A device as defined in claim 1 wherein said lower structure comprises: at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide or a conductive oxide film, and a metal plating layer disposed on and adhering to said at least one layer.

21. A semiconductor device comprising:

a substrate having a doped semiconductor region, a layered gate member, a lower conductor structure, an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure, and an upper conductor structure connected to said lower conductor structure via said through opening, wherein said upper structure comprises: an electroplated or electrolessly plated metal plating layer formed in said through opening; and a conductor structure component formed on said metal plating layer and on said insulating layer.

22. A device as defined in claim 21 wherein said conductor structure component is composed of two-layers, with at least one of the two layers being a further metal plating layer.